CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A content addressable memory (CAM) device, comprising:

a plurality of CAM arrays, each having a plurality of CAM cells;

a plurality of first priority encoders, each one of said first priority encoders being coupled to a respective one of said plurality of CAM arrays;

at least one subsequent priority encoder coupled to said plurality of first priority encoders, said subsequent priority encoder receiving outputs from said plurality of first priority encoders and selecting one of said outputs; and

a control circuit coupled to said plurality of CAM arrays, said plurality of first priority encoders, and said at least one subsequent priority encoder,

wherein said control circuit operates said plurality of CAM arrays so that at least a first one of said plurality of CAM arrays is operated in accordance with a first clock domain and at least a second one of said plurality of CAM arrays is operated in accordance with a second different clock domain.

2. The device of claim 1, wherein said plurality of CAM arrays comprises first and second CAM arrays.

3. The device of claim 1, wherein said plurality of CAM array comprises first, second, third, and fourth CAM arrays.

4. The device of claim 3, wherein said first and second CAM arrays are operated in accordance with the first clock domain and said third and fourth CAM arrays are operated in accordance with the second clock domain.

5. The device of claim 4, wherein said at least one subsequent priority encoder comprises:

a first subsequent priority encoder, coupled to said first and second CAM arrays;

a second subsequent priority encoder, coupled to said third and fourth CAM arrays; and

a third subsequent priority encoder coupled to outputs of said first and second subsequent priority encoder.

6. The device of claim 1, wherein said first clock domain and said second clock domain correspond to respective first and second clock signals which are supplied to said device.

7. The device of claim 6, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle.

8. The device of claim 7, wherein said second clock domain is delayed by one half clock cycle from said first clock domain.

9. The device of claim 1, wherein said first clock domain corresponds to a first clock signal and said second clock domain is corresponds to a second clock signal, said first and second clock signals being generated by the control circuit from a master clock signal supplied to said device.

10. The device of claim 9, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle.

11. The device of claim 10, wherein said second clock domain is delayed by one half clock cycle from said first clock domain.

12. The device of claim 1, further comprising at least one comparand register, wherein each of said at least one comparand register is coupled to the control circuit and wherein said at least one comparand register supplies a match pattern to said plurality of CAM arrays.

13. A processor based system, comprising:

a processor; and

a memory subsystem, coupled to said processor, said memory subsystem further comprising at least one content addressable memory (CAM) device, wherein at least one of said at least one CAM device further comprises,

a plurality of CAM arrays, each having a plurality of CAM cells;

a plurality of first priority encoders, each one of said first priority encoders being coupled to a respective one of said plurality of CAM arrays;

at least one subsequent priority encoder coupled to said plurality of first priority encoders, said subsequent priority encoder receiving outputs from said plurality of first priority encoders and selecting one of said outputs; and

a control circuit coupled to said plurality of CAM arrays, said plurality of first priority encoders, and said at least one subsequent priority encoder,

wherein said control circuit operates said plurality of CAM arrays so that at least a first one of said plurality of CAM arrays is operated in accordance with a first clock domain and at least a second one of said plurality of CAM arrays is operated in accordance with a second different clock domain.

14. The system of claim 13, wherein said plurality of CAM arrays comprises first and second CAM arrays.

15. The system of claim 13, wherein said plurality of CAM array comprises first, second, third, and fourth CAM arrays.

16. The system of claim 15, wherein said first and second CAM arrays are operated in accordance with the first clock domain and said third and fourth CAM arrays are operated in accordance with the second clock domain.

17. The system of claim 16, wherein said at least one subsequent priority encoder comprises:

a first subsequent priority encoder, coupled to said first and second CAM arrays;

a second subsequent priority encoder, coupled to said third and fourth CAM arrays; and

a third subsequent priority encoder coupled to outputs of said first and second subsequent priority encoder.

18. The system of claim 13, wherein said first clock domain and said second clock domain correspond to respective first and second clock signals which are supplied to said device.

19. The system of claim 18, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle

20. The system of claim 19, wherein said second clock domain is delayed by one half clock cycle from said first clock domain.

21. The system of claim 13, wherein said first clock domain corresponds to a first clock signal and said second clock domain is corresponds to a second clock signal, said first and second clock signals being generated by the control circuit from a master clock signal supplied to said device.

22. The system of claim 21, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle.

23. The system of claim 22, wherein said second clock domain is delayed by one half clock cycle from said first clock domain.

24. The system of claim 13, further comprising at least one comparand register, wherein each of said at least one comparand register is coupled to the control circuitry and wherein said at least one comparand register supplies a match pattern to said plurality of CAM arrays.

25. A method for operating a content addressable memory (CAM) device, comprising:

controlling a search operation of at least a first CAM array in accordance with a first clock signal; and

controlling a search operation of at least a second CAM array in accordance with a second clock signal,

wherein said first and second clock signals are different.

26. The method of claim 25, further comprising the steps of:

receiving said first clock signal as a master clock signal supplied to said device; and

generating said second clock signal from said first clock signal.

27. The method of claim 26, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle.

28. The method of claim 27, wherein said second clock signal is said first clock signal delayed by one half cycle.

29. The method of claim 26, further comprising the steps of:

receiving said first clock signal from an external source; and

receiving said second clock signal from the external source.

30. The method of claim 24, wherein said second clock domain is offset from said first clock domain by any fractional clock cycle.

31. The method of claim 30, wherein said second clock signal is equal to said first clock signal delayed by one half cycle.

32. The method of claim 25, further comprising the steps of:

selecting a first intermediate match from said at least a first CAM array;

selecting a second intermediate match from said at least a second CAM array; and

selecting one of said first intermediate match and said second intermediate match asn an output.

33. A router, comprising:

a processor;

a first network interface, coupled to said processor;

a second network interface, coupled to said processor; and

a memory subsystem, coupled to said processor, said memory subsystem further comprising at least one content addressable memory (CAM) device, wherein at least one of said at least one CAM device further comprises:

a plurality of CAM arrays, each having a plurality of CAM cells;

a plurality of first priority encoders, each one of said first priority encoders being coupled to a respective one of said plurality of CAM arrays;

at least one subsequent priority encoder coupled to said plurality of first priority encoders, said subsequent priority encoder receiving outputs from said plurality of first priority encoders and selecting one of said outputs; and

a control circuit coupled to said plurality of CAM arrays, said plurality of first priority encoders, and said at least one subsequent priority encoder,

wherein said control circuit operates said plurality of CAM arrays so that at least a first one of said plurality of CAM arrays is operated in accordance with a first clock domain and at least a second one of said plurality of CAM arrays is operated in accordance with a second different clock domain; and

wherein said processor searches a routing table stored in said memory subsystem to route packets between said first and second network interfaces.